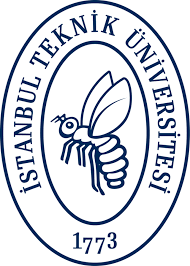
****

**DIGITAL SYSTEM DESIGN APPLICATION – EHB 436E**

**Experiment III**

**Yiğit Bektaş GÜRSOY**

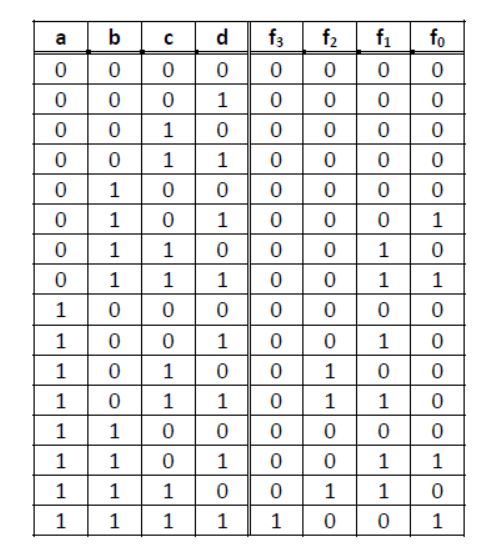
**040180063**

**Class Lecturer: Sıddıka Berna Örs Yalçın**

**Class Assistant:  
Serdar Duran  
Yasin Fırat Kula  
Mehmet Onur Demirtürk**

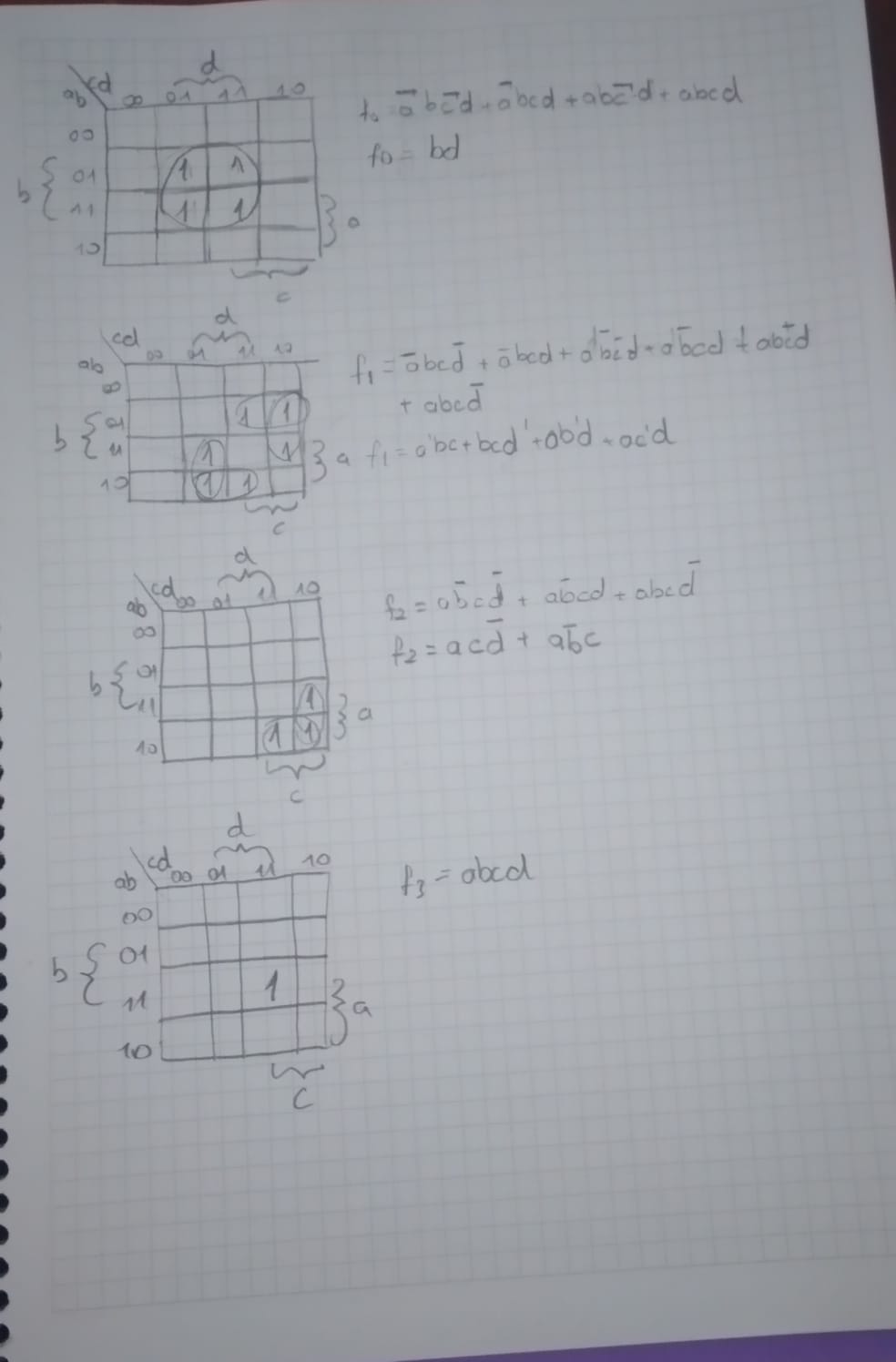
1. **REALIZATION WITH SSI LIBRARY**

* We have a truth table as indicated in the image below

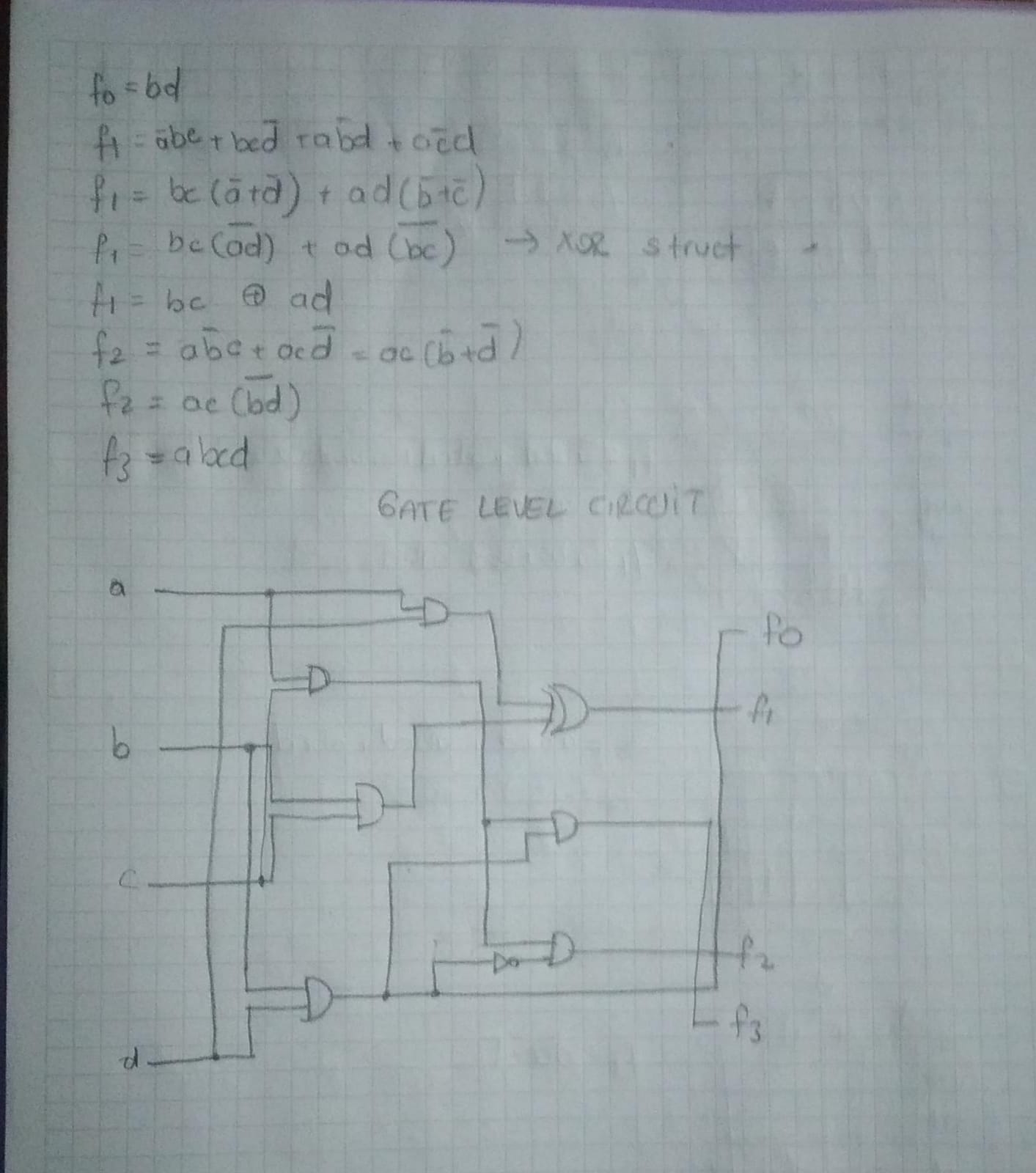


* We can write this function in its simplest form with the karnaugh map method we learned in logic circuits.

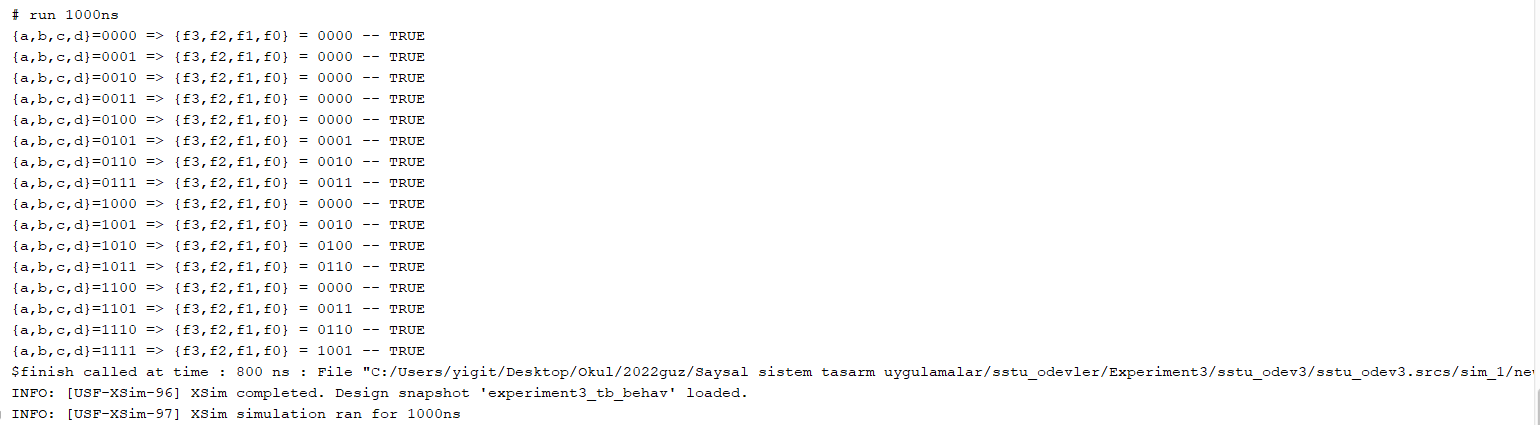
**Reduction with Karnough MAP**

****

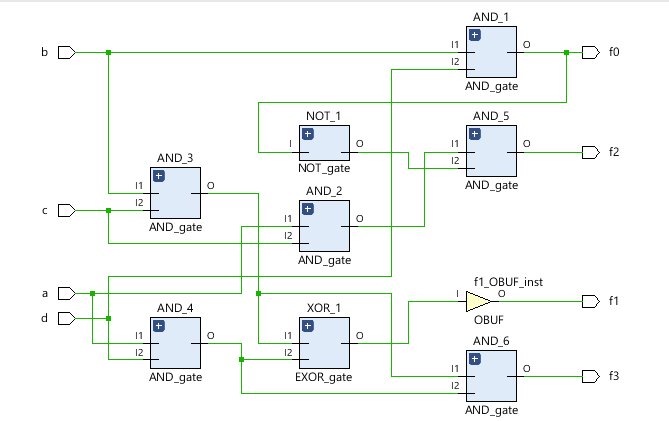
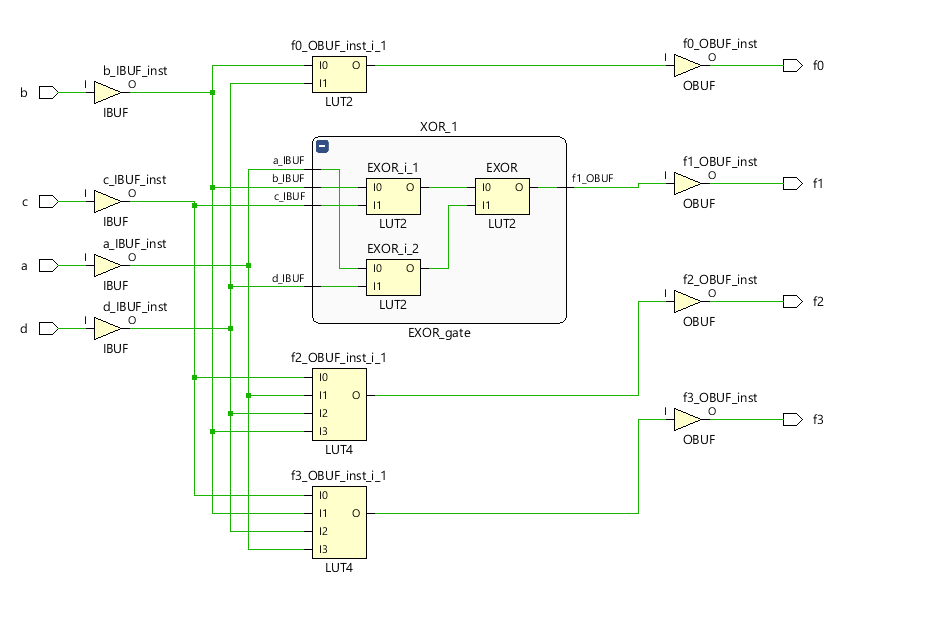
**Boolean expressions of the function and Gate Level Circuit**

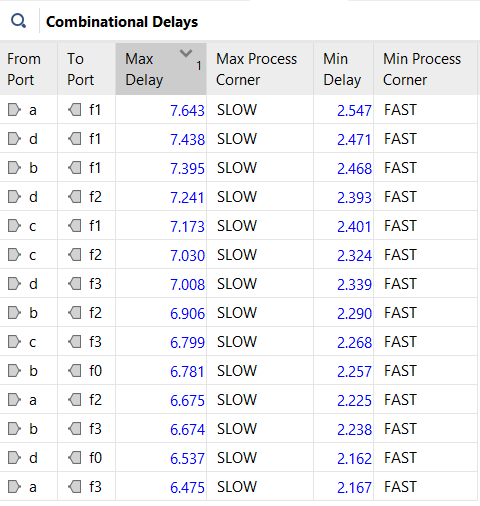
****

**BEHAVIORAL SIMULATION**

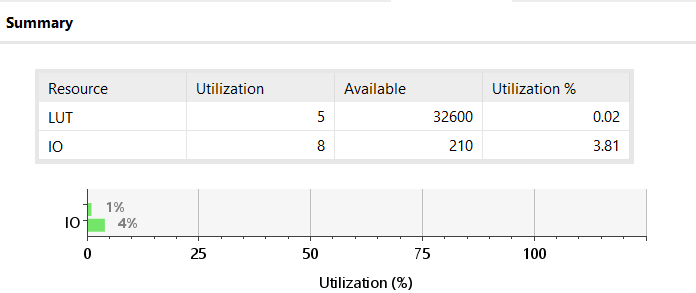
* ****TCL Console output is given below.

**Design with NO Constraints**

* RTL Schematic
* Technology Schematic
* Path Delays



* Utilization Summary

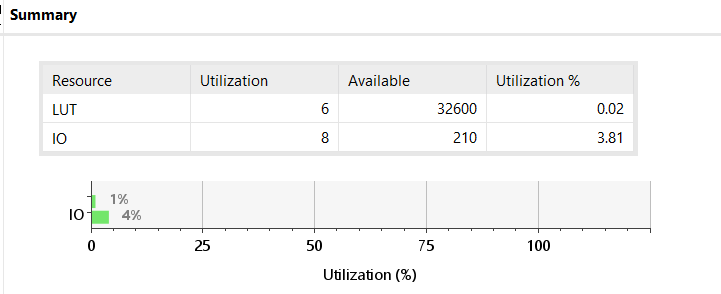
****

**Design with Time Constraints**

* Path Delays
* As seen in the photo above, I saw delays close to and above 7ns, so I set the time constraints maximum delay to 7ns. The results are as follows.

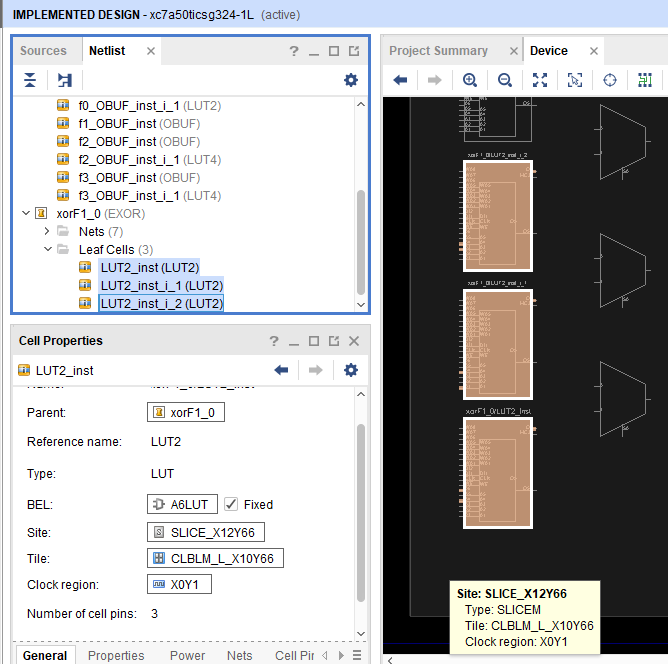
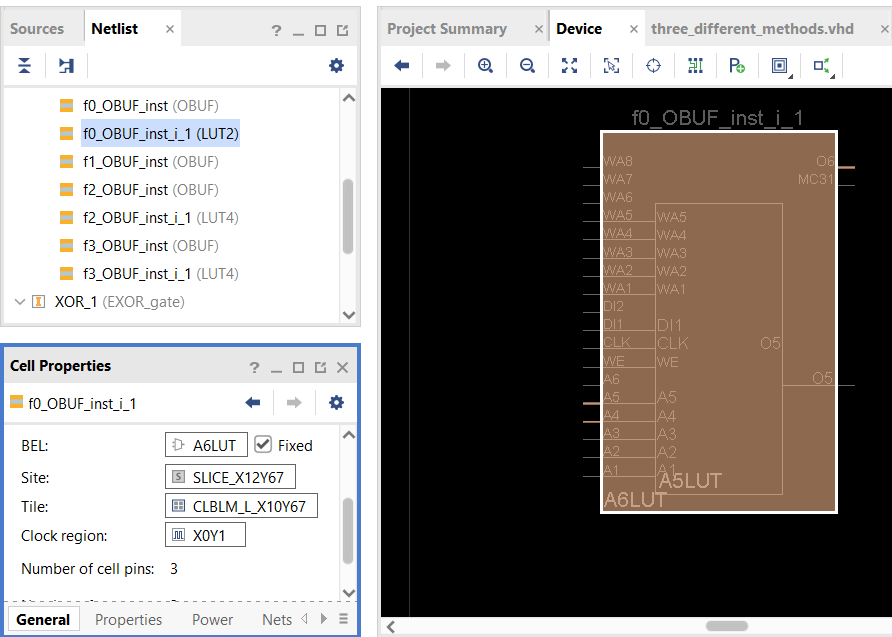
****

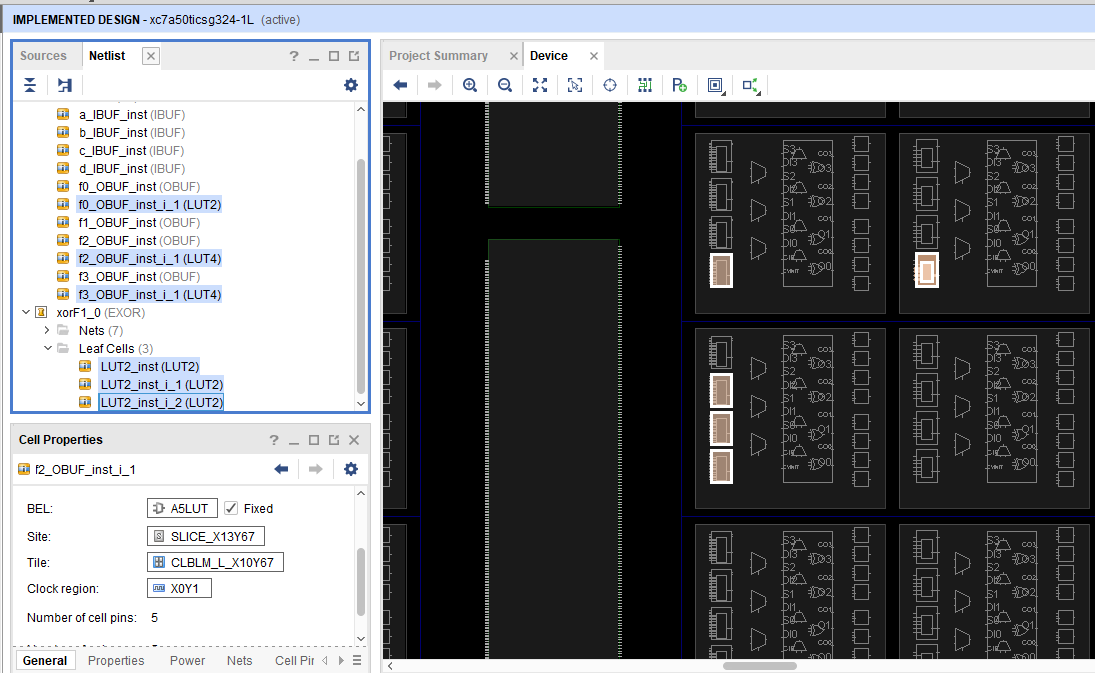
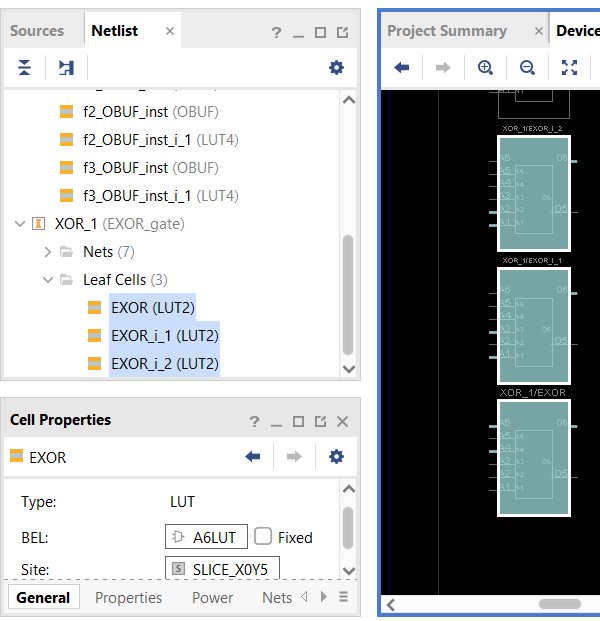
* Utilization Summary
* If we look at the previous utilization summary, this result is 1 LUT more.

****

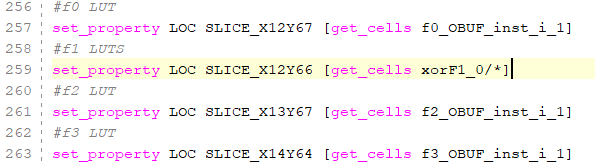
**Design with LOC Constraints**

* Placement f0,f1,f2,f3 respectively.

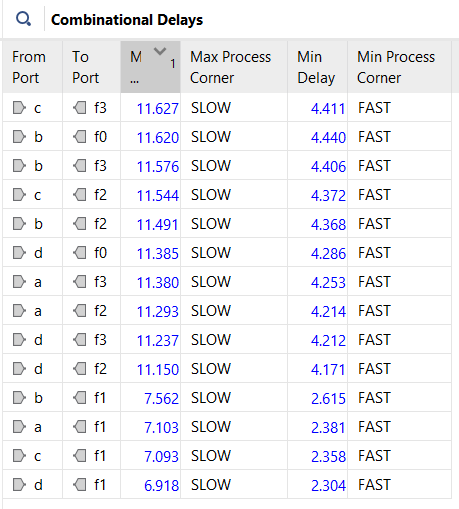


****

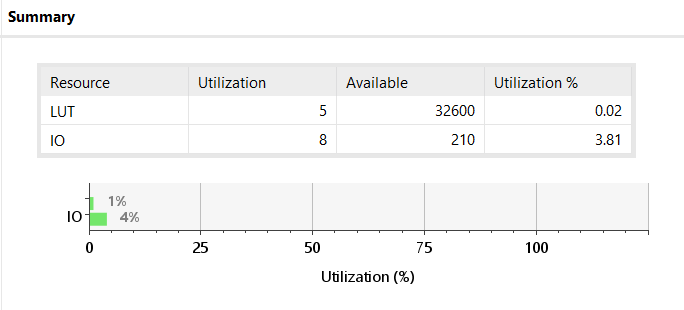
* Placed the LUTs on the device as stated in the assignment. As a result of these placements, our delays have almost doubled.

****

* Path Delays

****

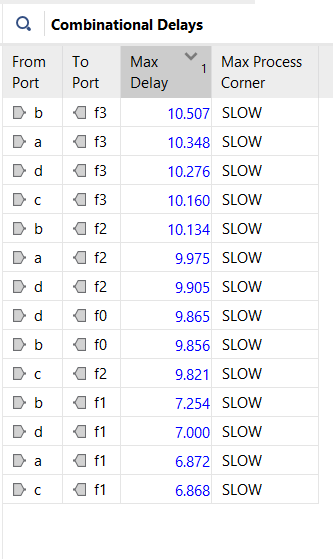
* Utilization



**Design with Time ( LOC CONSTRAINTS)**

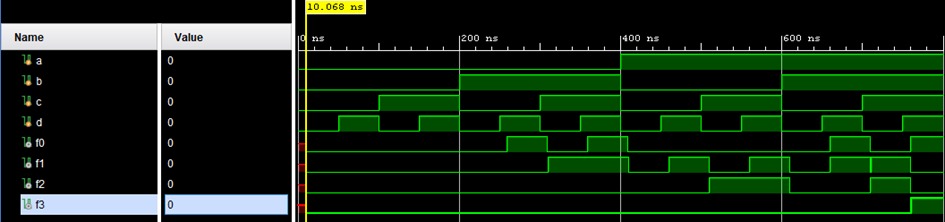
* Path Delays

I tried to reduce the maximum delay below 10ns. The output of my operation is as follows.

****

* Post-implementation Timing Simulation

The red line above shows that there is a delay due to setup and hold time.



**CONCLUSION**

Implementation : Max Time Delay (ns)

Without any constraints : 7.643

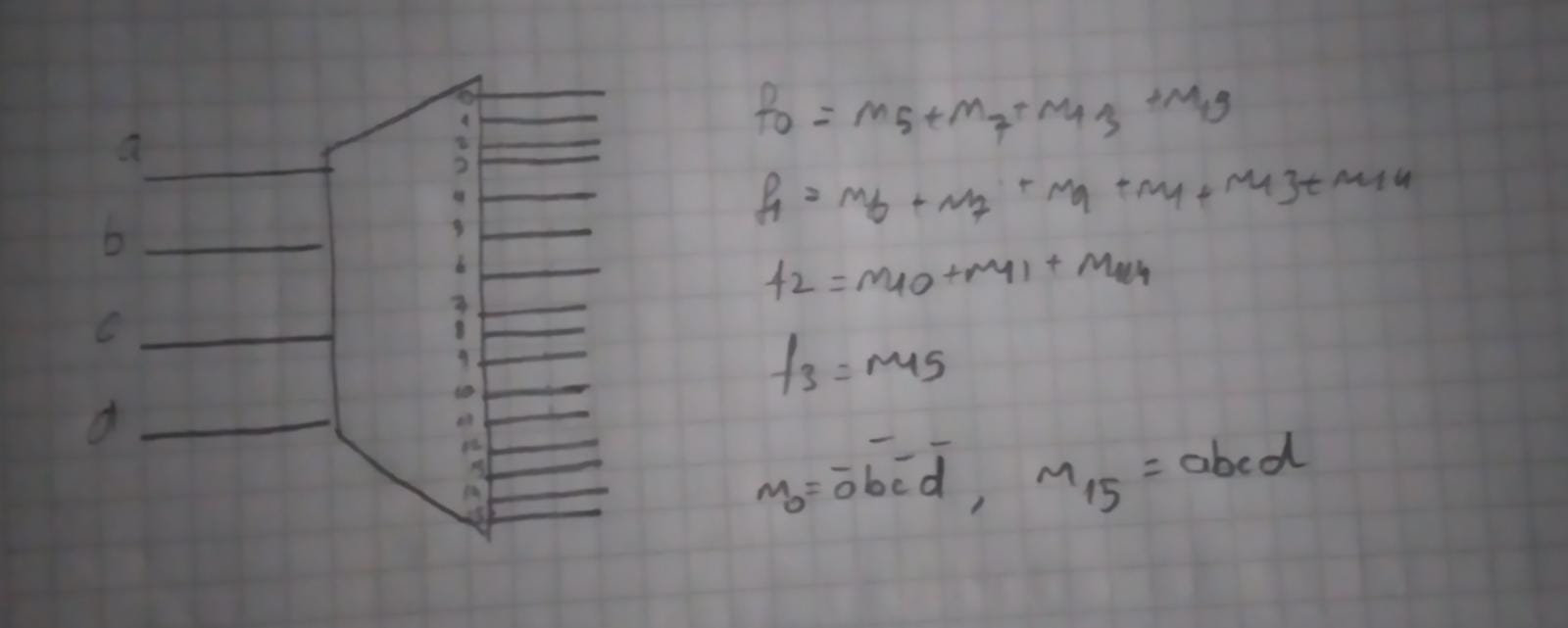
With time constraints (7ns) : 6.907

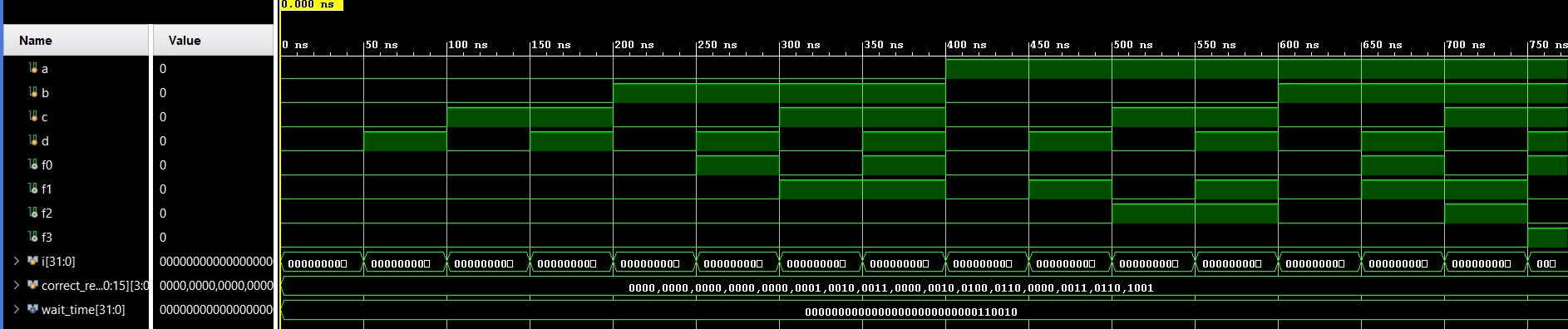
With LOC constraints : 11.627

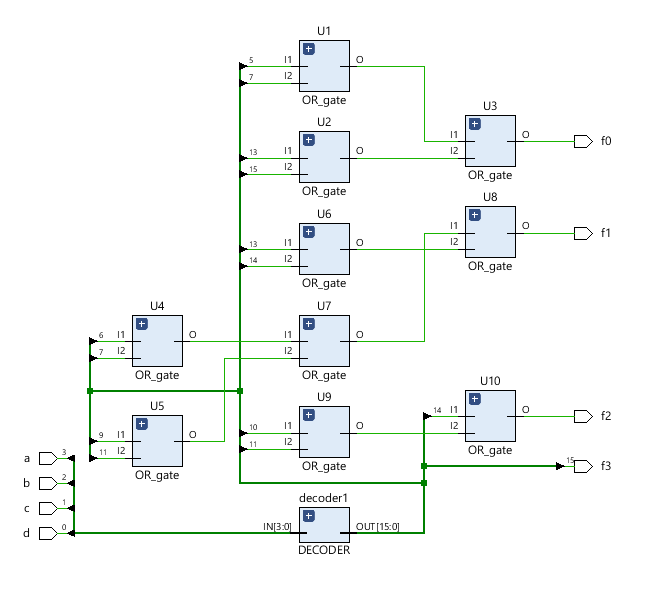
With time LOC constraints and set max delay (10ns) : 10.507

1. **REALIZATION WITH DECODER**

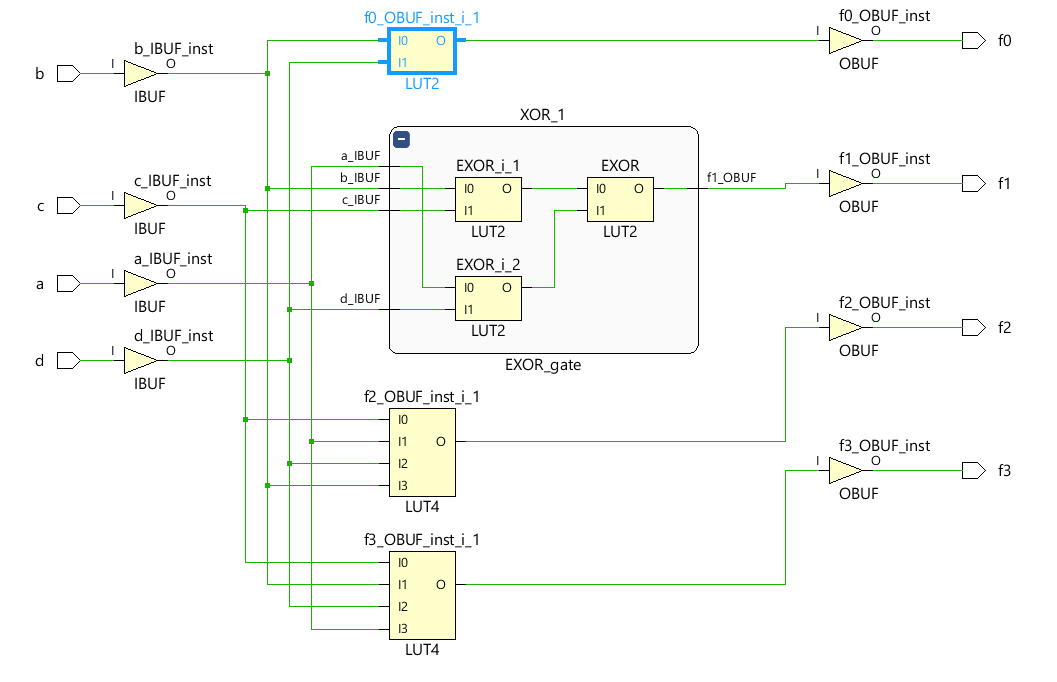
**4x16 Decoder Representation**



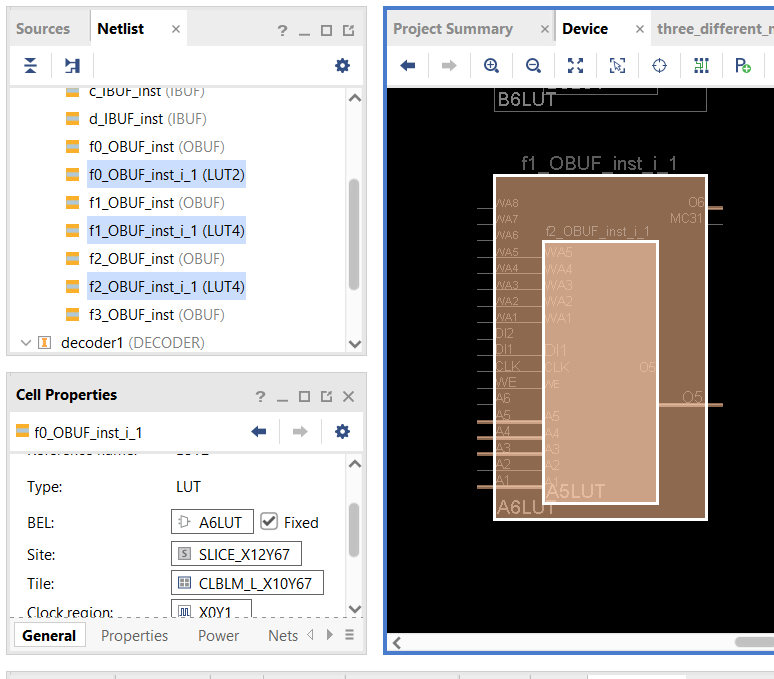
* Behavioral Simulation
* RTL Schematic



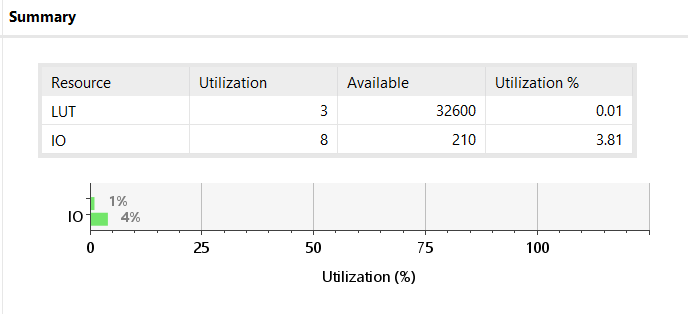
* Technology Schematic

****

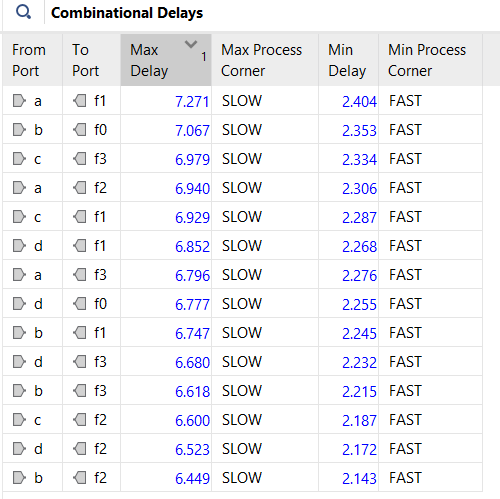
* Device Placement



* Utilization Summary



* Path Delay
* No time constraints

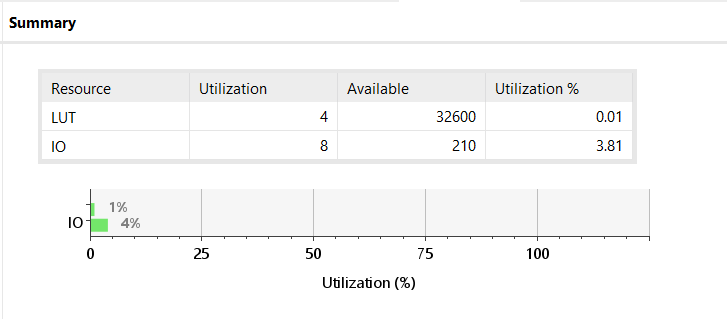


* Adding time constraints

Max delay is set to 7 ns time constraints.

****

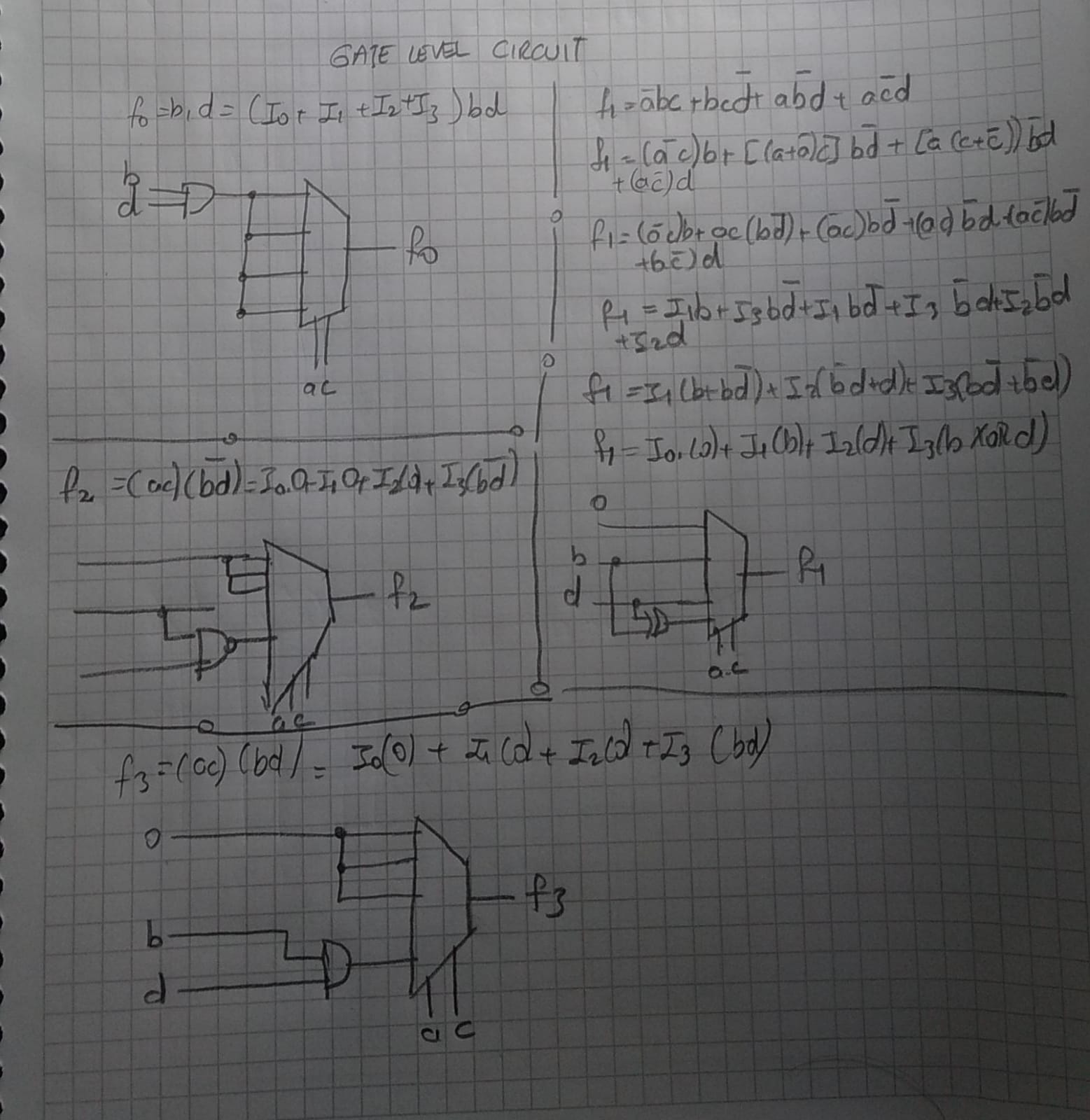
* Utilization Summary

****

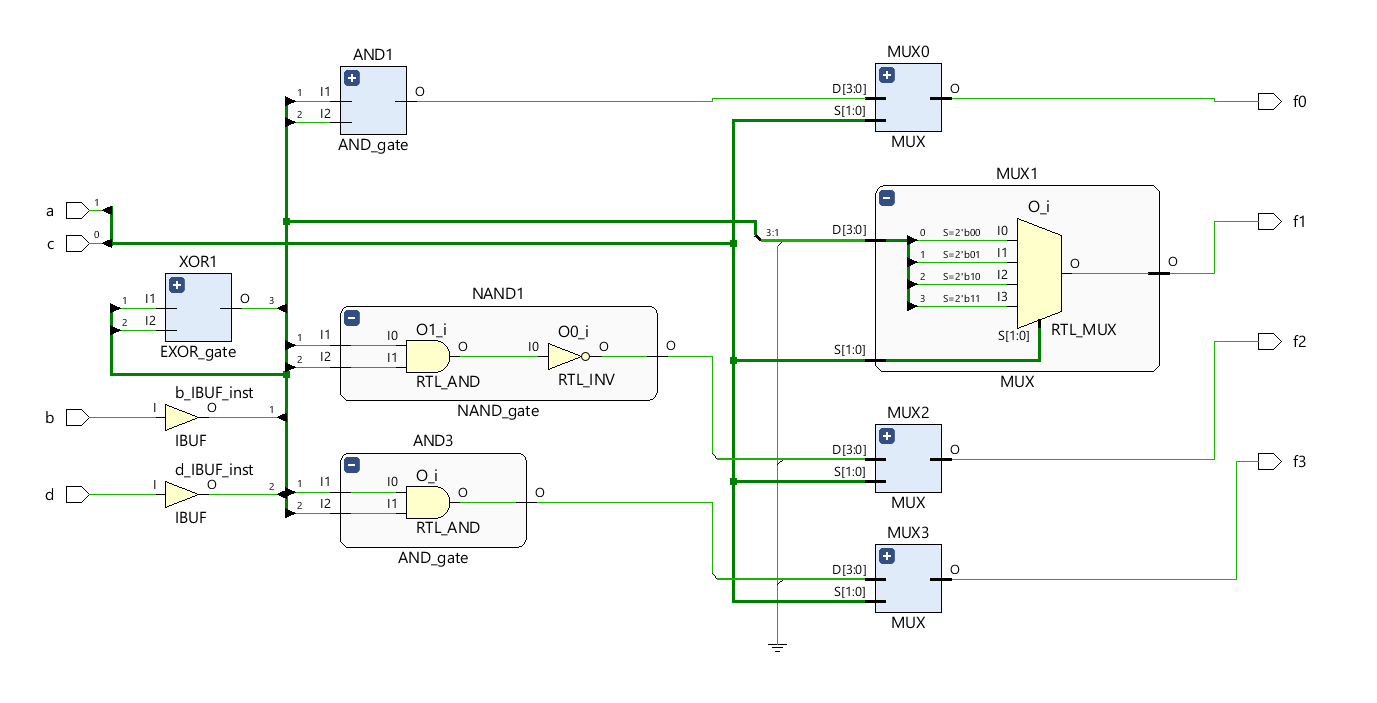
We reduced the delays below 7ns by adjusting the time constraint, but 1 LUT was added to our structure as an extra.

1. **REALIZATION WITH MUX**

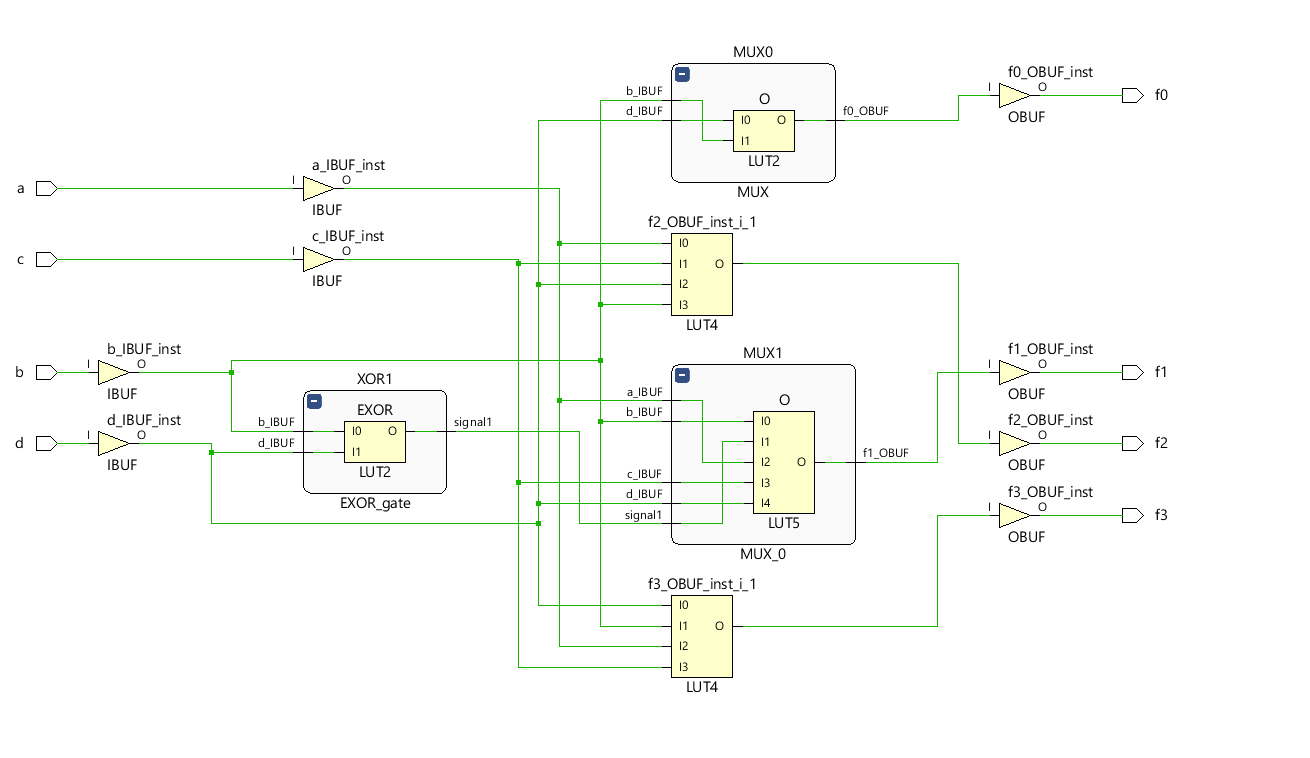
* Gate Level Circuit



* RTL Schematic

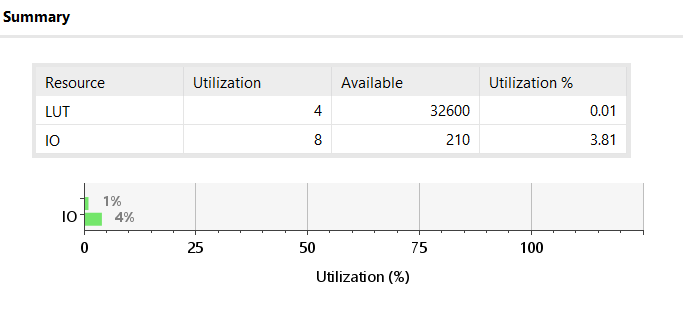


* Technology Schematic

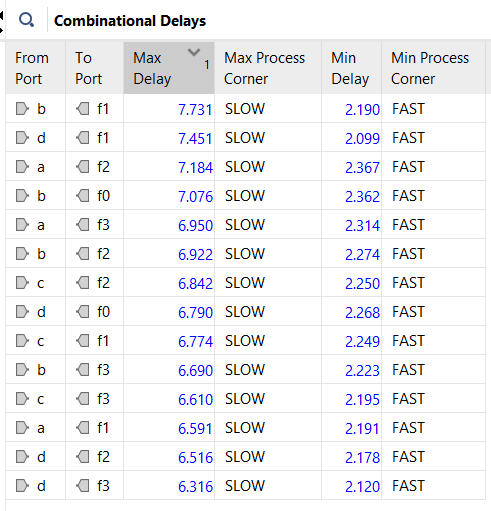


I saw the LUT5 build here, which I hadn't seen in previous assignments. LUT5 is a LookUpTable with 5 inputs and 1 output.

* Utilization Summary



* Path Delays
* No time constraints

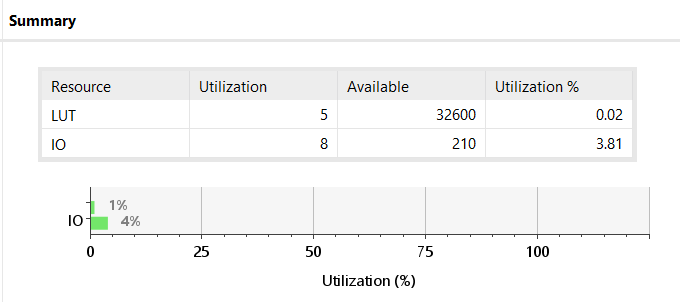


* With time constraints

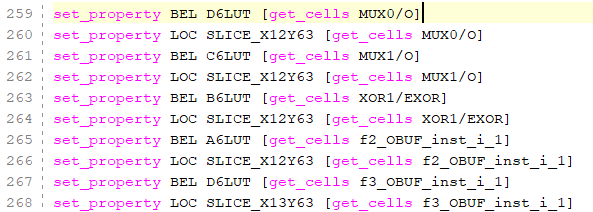
With time constraints it is achieved to get below 7ns time constraints. Results are given below.

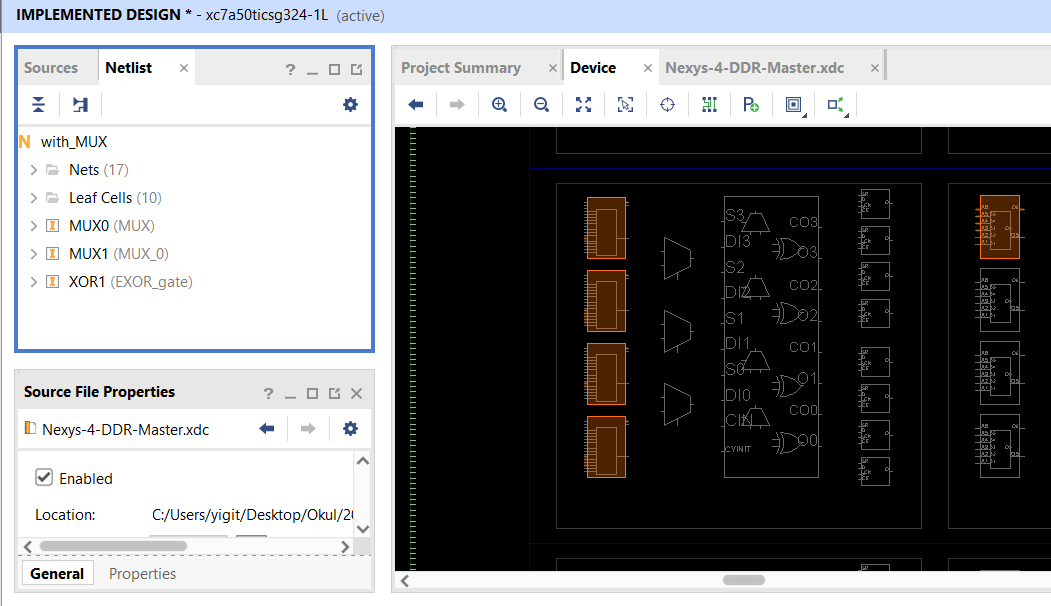


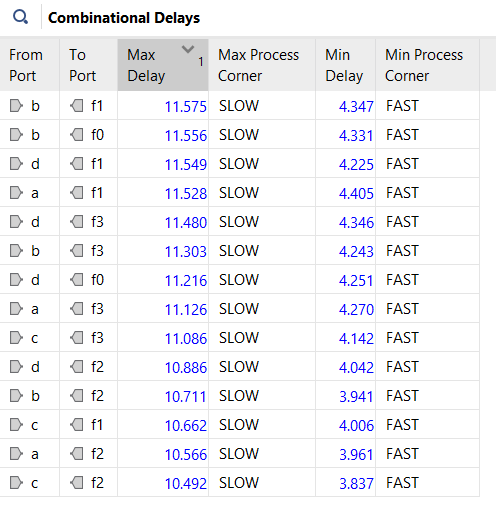
* Utilization Summary



* Device placement and Combinational Delays





****

* Our combinational delays have increased noticeably due to random placement of locations within the device. The relevant outputs are shown in the figure above.

**LUT Usage**

Decoder : 3 (Best LUT Usage)

MUX : 4

SSI: 5 (Worst LUT Usage)

**Path Delays**

Decoder : 7.271ns (Best delay)

MUX : 7.731ns (Worst delay)

SSI : 7.643ns

**Final comments**

* Decoder is the simpliler than the other structures , with\_SSI and MUX, it is need to be used the decoder and OR\_gates the necessary outputs together..
* MUX is more complex to design than the other structures , with\_SSI and MUX, the design of the design was more difficult to think through and more time was spent than others.
* If we look at the coding side, I used less submodules in the MUX structure compared to other modules, while the decoder was the structure where I used the most submodules.